Remarks

Claims 1-14 are pending in the Office action. Claims 1-9 have been allowed. Claims 10-14 have been rejected. Claims 10 and 14 have been amended to recite sufficient antecedent basis for claim limitations. Reconsideration of the rejected claims is respectfully requested.

Rejections Under 35 U.S.C. § 112

The limitation of claim 10 reciting "the security row" has been amended to recite "a security row". Therefore, the rejection to claim 10 should be withdrawn.

The limitation of claim 14 reciting "said lockbit sense amplifier" has been amended to recite "a lockbit sense amplifier". Therefore, the rejection to claim 14 should be withdrawn.

Claims 11-14 were rejected for depending and including the limitations of claim 10. As the rejection to claim 10 should be withdrawn for at least the reason provided above, so should the rejections to dependent claims 11-14.

Rejections Under 35 U.S.C. § 102

Claims 10 and 11 were rejected under 35 U.S.C. § 102(b) as being anticipated by Usami et al. This rejection is respectfully traversed.

In rejecting the claims, the Examiner states:

> Regarding claim 10, Usami discloses a method of operating an embedded semiconductor memory (memories 51, 52 embedded in MCU chip 2) comprising: having security lock protection responsive [to] an external access request to said memory (column 5); and disabling external access to a memory array row whenever a security bit (2-bit security bit; column 4, lines 27) in the security row indicates locked status, and otherwise enabling access to the memory array (with A=1 and B=1; column 5, lines 46-53).

Applicant respectfully submits that in Applicant's claimed invention a single bit indicates a locked status. Specifically, Applicant's claim 10 recites in pertinent part, "disabling external access to a memory array row whenever a security bit in a security row indicates a locked status…."

In contrast, in Usami two bits, not a single bit, are utilized and required to prohibit external access to the main memory. Usami fails to teach or suggest that one bit can be used to indicate a locked status disabling external access to a memory array row as claimed in Applicant's invention. Nothing in Usami suggests that the use of two bits is optional.

In the quote above, the Examiner appears to equate a single security bit capable of indicating a locked status (as recited in Applicant's claim 10) with a 2-bit lock (as recited in the cited Usami reference). However, a single security bit that is capable of indicating a locked status is different from two bits. Though two bits may perform a particular function, it does not necessarily follow that one bit would perform the same function as two. Therefore, for at least this reason, Usami fails to teach or suggest elements of Applicant's claim 10.

Further, Applicant submits that if the two bits disclosed in Usami were modified to one bit, a principle of operation of Usami would be modified. Specifically, Usami discloses the use of two bits stored by transistors A and B to indicate the following:

1. prohibition of an external write to and read from the main memory and enablement of external write to the auxiliary memory (A=0 and B=0);
2. prohibition of an external write to and read from the main memory and disablement of a write to the auxiliary memory (A=1 and B=1); and

3. permitting an external write to and read from the main memory and permitting a write to the auxiliary memory (A=1 and B=0) or (A=0 and B=1).

Thus, it is clear that two bit states are required in Usami in order to make the various determinations with regard to reading or writing. One bit is not disclosed as being sufficient to make such determinations. The M.P.E.P. explicitly states that "[i]f the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious." M.P.E.P. § 2143.01, 2100-132 (Rev 2, May 2004) (citing *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)). Here, the proposed modification of Usami would change the principle of operation of Usami. Therefore, the teachings of Usami are not sufficient to render Applicant's claim 10 obvious. Accordingly, withdrawal of the rejection to claim 10 is respectfully requested.

Claims 11-14 depend from claim 10, therefore, the rejection to these claims should be withdrawn for at least the same reasons as claim 10.

Allowable Subject Matter

The Examiner has indicated that claims 1-9 are allowed.

The Examiner has also indicated that claims 12-14 would be allowed if amended to include all of the limitations of the base claim and any intervening claims. In response, Applicant submits that claim 10 should be allowed for at least the reasons provided above. Therefore, Applicant submits that dependent claims 11-14 are allowable for at least the same reasons as claim 10.

Conclusion

For at least the reasons submitted above, Applicant respectfully submits that the claims are in condition for allowance. Accordingly, a Notice of Allowance is respectfully requested.

CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signed: Sally Azevedo
Typed Name: Sally Azevedo

Date: November 3, 2004

Respectfully submitted,

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